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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/210,545	12/14/1998	KATSUHISA OGAWA	35.C13212	5262

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EXAMINER	
GENCO, BRIAN C	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/210,545	OGAWA ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 24, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 23, 2004 has been entered.

Applicant's arguments filed January 24, 2006 have been fully considered but they are not persuasive.

Applicant argues that Chen does not disclose a processing circuit which processes the output lines, and therefor fails to teach that the processing circuit functions together with the block memory as required by Applicant's claims.

In response, Examiner notes that there is no limitation that the "processing circuit functions together with the block memory". Further, Examiner notes Chen's disclosure that the three pixels are lumped together as one composite pixel wherein there is inherently an operation section as claimed so as to lump the pixels together.

Applicant argues that Miyawaki does not disclose an input structure of a processing circuit "as acknowledged by the Examiner in the Office Action (page 6, the last two lines)".

In response, Examiner notes that in continuing that same paragraph that on page 7, the first two lines, the Examiner has provided a citation by Miyawaki indicating that the signals may be input to an image processing unit in parallel.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by (USPN 4,658,287 to Chen).

In regards to claim 23 Chen discloses an image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements (e.g., Fig. 1 wherein a pixel block comprises the three photo-detection elements 10, 20, and 22);

a plurality of output lines which output, in parallel, signals of the photo-detection elements included in the block (e.g., elements 57-59 of Fig. 1); and

an operation section which receives as inputs, in parallel, and in relation to one of said blocks to be subjected to operation, the signals of corresponding predetermined ones of said plurality of blocks which are outputted in parallel from said plurality of output lines, wherein said operation section performs an interpolation processing to interpolate a predetermined signal using signals other than the predetermined signal (e.g., column 7, line 61 – column 8, line 36 wherein it is disclosed the three pixels in a pixel block form a composite pixel. The Examiner interprets the operation used in Chen to be an interpolation operation since one pixel values is generated from a combination of the three color values).

In regards to claim 25 Chen discloses an image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements (e.g., Fig. 1 wherein a pixel block comprises the three photo-detection elements 10, 20, and 22);

a plurality of output lines which output, in parallel, signals of the photo-detection elements included in the block (e.g., elements 57-59 of Fig. 1); and

an operation section which receives as inputs, in parallel and in relation to one of said blocks to be subjected to operation, the signals of corresponding predetermined ones of said plurality of blocks which are outputted in parallel from said plurality of output lines, wherein said operation section performs a compression processing (e.g., column 7, line 61 – column 8, line 36 wherein it is disclosed the three pixels in a pixel block form a composite pixel, wherein this interpolation is a compression processing).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,658,287 to Chen) in view of (USPN 5,196,939 to Elabd et al).

In regards to claim 24 Chen discloses an image pickup element according to claim 23, wherein said pixel area includes a plurality of partial pixel-areas (e.g., pixel block trio's shown in Fig. 1) arranged two-dimensionally in horizontal and vertical directions (e.g., Fig. 1), and

wherein each of the plurality of partial pixel-areas include photodetectors arranged two-dimensionally in the horizontal and vertical directions (e.g., elements 10, 20, and 22 are two-dimensionally arranged in the horizontal and vertical directions);

Chen does not disclose nor preclude said image pickup element further comprises a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction, and a selecting circuit which reads out the signals in parallel from the memory to said plurality of output lines on a partial pixel-area basis.

Elabd discloses said image pickup element further comprising a memory which stores signals of a plurality of lines of the photodetectors arranged in the horizontal direction (e.g., element 33 of Fig. 4 wherein the storage element 33 holds a predetermined number of rows; column 5, lines 35-37), and a selecting circuit which reads out the signals in parallel from said memory to a plurality of output lines on a partial pixel-area basis (e.g., the dump drain 35 drains the unselected signals in the memory and outputs the selected ones, wherein the selected lines are in a partial pixel-area basis as shown in Fig. 2B). This enables the selection of a desired block of data from within the image as shown in Fig. 2B. Therefore it would have been obvious to one skilled in the art at the time of the invention to have added Elabd's storage and selection circuits to Chen's invention in order to enable the selection of an area of interest from within the image as shown in Fig. 2B.

In regards to claim 26 see examiners notes on the rejection of claims 24 and 25.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,658,287 to Chen) in view of (USPN 6,014,467 to Asano).

In regards to claim 27 Chen discloses an operation section through the provision of creating the composite pixel. Chen does not disclose nor preclude the operation section which inputs, in parallel, the signals outputted in parallel from said plurality of output lines, wherein said operation section performs a discrete cosine transform (DCT).

Asano discloses a DCT unit, element 2 of Fig. 1, which inputs 8x8 blocks of image data to the DCT in parallel (column 4, lines 48 – column 5, line 4). Such image processing clearly provides for more effective data storage and transmission, as is well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have stored the composite image data of Chen in Asano's image memory so as to performed DCT post-processing in order to put the image data into a standardized compressed format such as JPEG and to enable more efficient data storage and transmission.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,658,287 to Chen) in view of (USPN 4,816,910 to Hashimoto et al).

In regards to claim 28 see Examiners notes on the rejection of claims 23 and 25.

Chen does not disclose nor preclude an operation section which receives as inputs, in parallel and in relation to one of said blocks to be subjected to operation, signals of corresponding predetermined ones of said plurality of blocks, originating from the signals outputted in parallel from said plurality of output lines, wherein said operation section performs edge-emphasis processing. Hashimoto et al, herein Hashimoto, discloses outputting image data in parallel from an image sensor to an edge emphasis processor, or edge enhancement means (claims 6-8 on column 11, line 51 – column 12, line 8). Therefore it would have been obvious to

one of ordinary skill in the art at the time of the invention to have had an edge emphasis processor at the output of Chen's image sensor in order to perform edge enhancement with a simplified structure as disclosed by Hashimoto (column 3, lines 15-27).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 4,658,287 to Chen) in view of (USPN 4,816,910 to Hashimoto et al) in further view of (USPN 5,196,939 to Elabd et al).

In regards to claim 29 see examiners notes on the rejection of claims 24, 26, and 28.

Claim 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,343 to Miyawaki et al.) in view of (USPN 6,181,376 to Rashkovskiy et al.).

In regards to claim 23 Miyawaki discloses an image pickup element formed on a single semiconductor chip, comprising:

a pixel area including an arrangement of a plurality of blocks, each block including at least two photo-detection elements (e.g., column 2, lines 48-53 and column 3, lines 14-17 wherein Examiner is defining the 2x2 pixel block shown in Fig. 1 as a pixel block, the image sensor being partitioned into a plurality of such blocks, column 3, lines 14-17);

a plurality of output lines which output, in parallel at the same time, signals of all of the photo-detection elements included in the block (e.g., column 3, lines 21-25; Fig. 1).

Miyawaki does not disclose nor preclude that the signals output in parallel are input in parallel where interpolation processing is applied to the signals. Examiner notes that Miyawaki

does disclose the ability to input the signals in parallel to an image processing unit (column 9, lines 37-40).

Examiner notes that it is extremely well known in the art to provide color filter arrays to an image sensor so as to generate a color image as disclosed in Fig. 1 of Rashkovskiy. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a color filter with Miyawaki's invention in order to generate a color image. Examiner further notes that it is extremely well known to provide interpolation for demosaicing a color filter in order to generate all of the color signals for each pixel location for complete color reproduction (column 1, line 35 – column 2, line 19; column 3, lines 33-39; column 4, lines 47-60; Rashkovskiy). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have used any of the demosaicing techniques disclosed by Rashkovskiy in order to generate all of the color signals for each pixel location for complete color reproduction and for generating an aesthetically pleasing display of the current scene.

In regards to claim 24 note column 2, lines 44-47; column 3, lines 20-25; and Figs. 1 and 2 of Miyawaki, in particular elements 111,112, 121, and 122.

Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,343 to Miyawaki et al.) in view of (USPN 6,014,467 to Asano).

In regards to claim 25 see Examiners notes on the rejection of claim 23. Miyawaki does not disclose nor preclude that the signals output in parallel are input in parallel where compression processing is applied to the signals.

Asano discloses performing compression processing to compress an image into JPEG format (e.g., column 4, lines 20-26). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed JPEG image compression on Miyawaki's image signals in order to generate a standardized compressed format and to enable more efficient data storage and transmission.. Asano further discloses a DCT unit, element 2 of Fig. 1, which inputs 8x8 blocks of image data to the DCT in parallel (column 4, lines 48 – column 5, line 4). Such image processing clearly provides for more effective data storage and transmission, as is well known in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have performed DCT post-processing in order to put the image data into a standardized compressed format and to enable more efficient data storage and transmission.

In regards to claim 26 see Examiners notes on the rejection of claims 24 and 25.

In regards to claim 27 see Examiners notes on the rejection of claim 25.

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,343 to Miyawaki et al.) in view of (USPN 4,816,910 to Hashimoto et al).

In regards to claim 28 see Examiners notes on the rejection of claim 23.

Miyawaki does not disclose nor preclude that the signals output in parallel are input in parallel where edge-emphasis processing is performed. Hashimoto et al, herein Hashimoto, discloses outputting image data in parallel from an image sensor to an edge emphasis processor, or edge enhancement means (claims 6-8 on column 11, line 51 – column 12, line 8). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have

had an edge emphasis processor at the output of Chen's image sensor in order to perform edge enhancement with a simplified structure as disclosed by Hashimoto (column 3, lines 15-27).

In regards to claim 29 see Examiners notes on the rejection of claim 24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 571-272-7364 or by fax at 571-273-7364. The examiner can normally be reached on Monday thru Friday 8:30am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached at 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian C Genco
Examiner
Art Unit 2615

March 29, 2005

TUAN HO
PRIMARY EXAMINER